

FIG. 1  
DATA NET

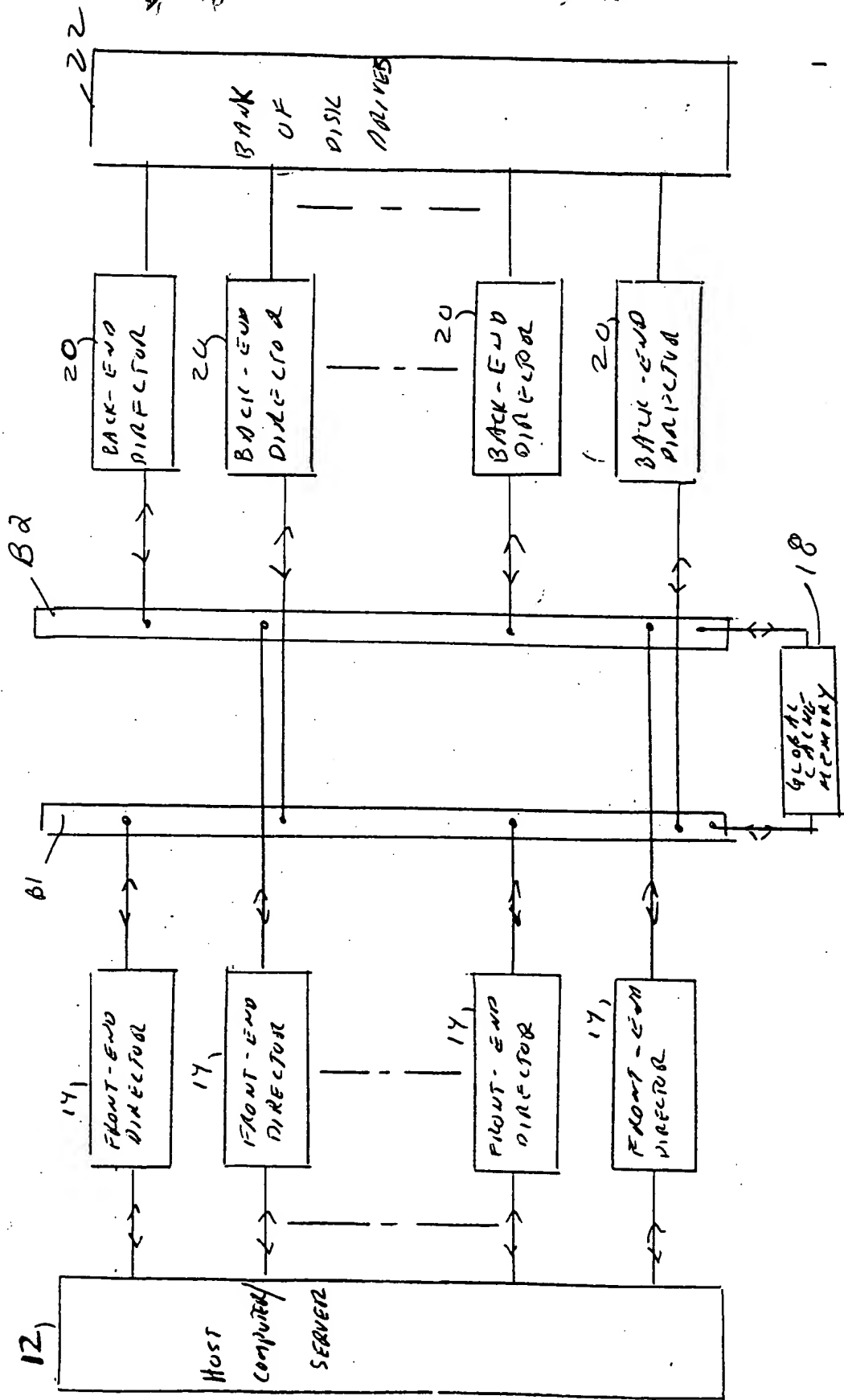




FIG. 3

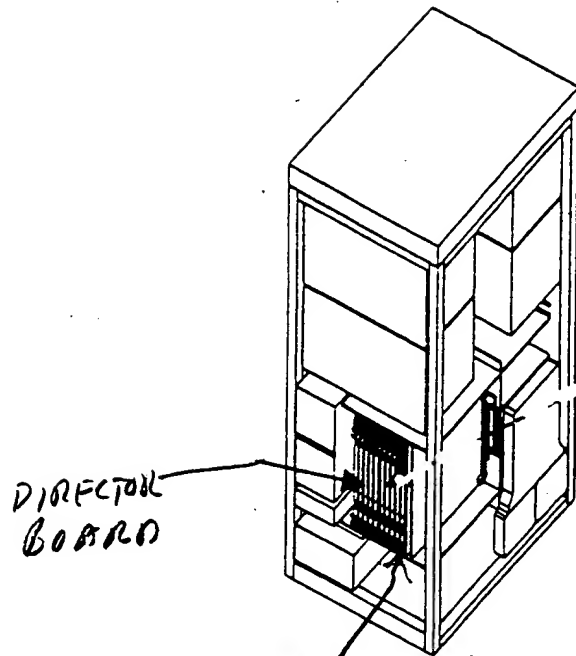


FIG. 4

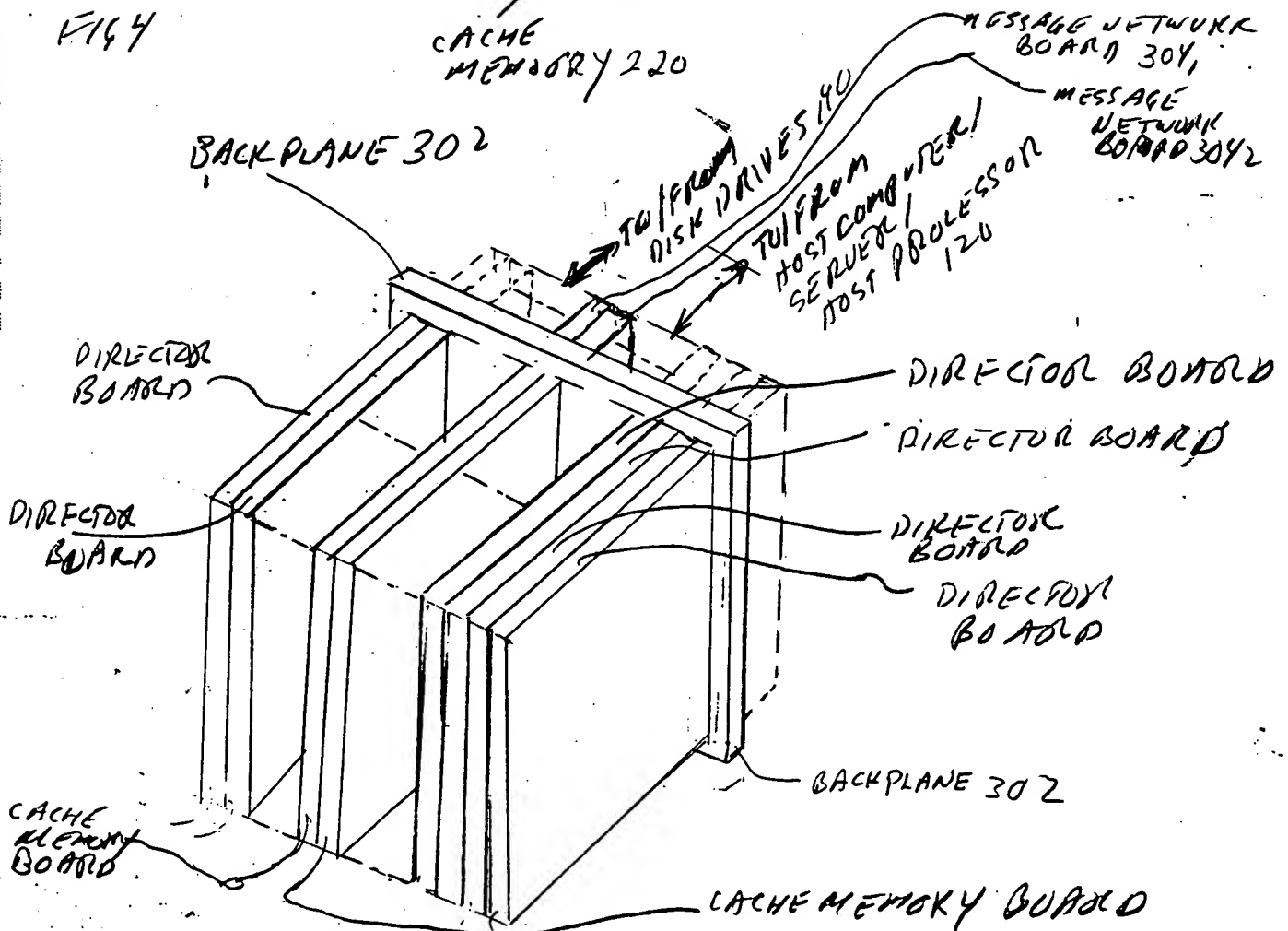
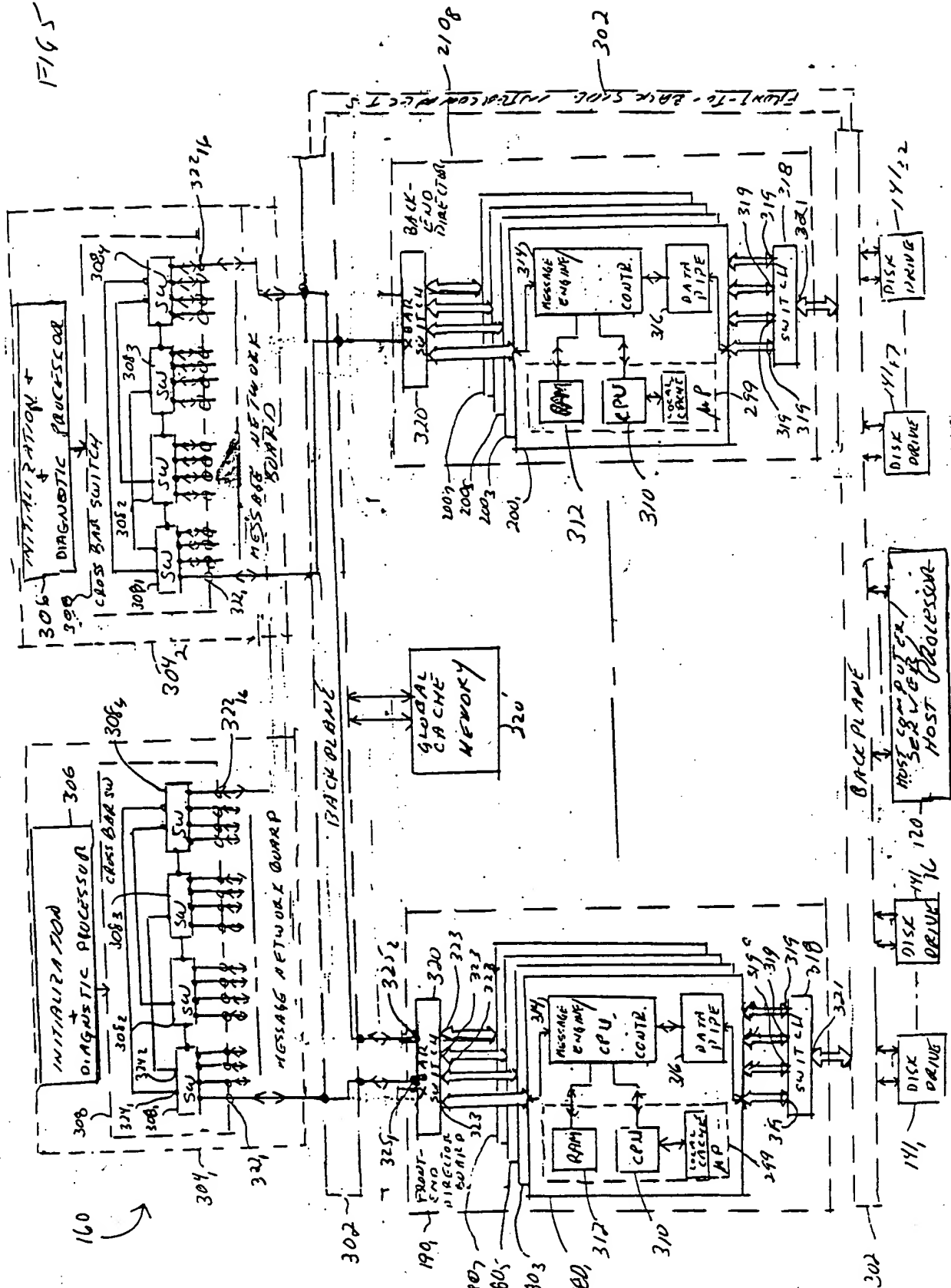


FIG 5



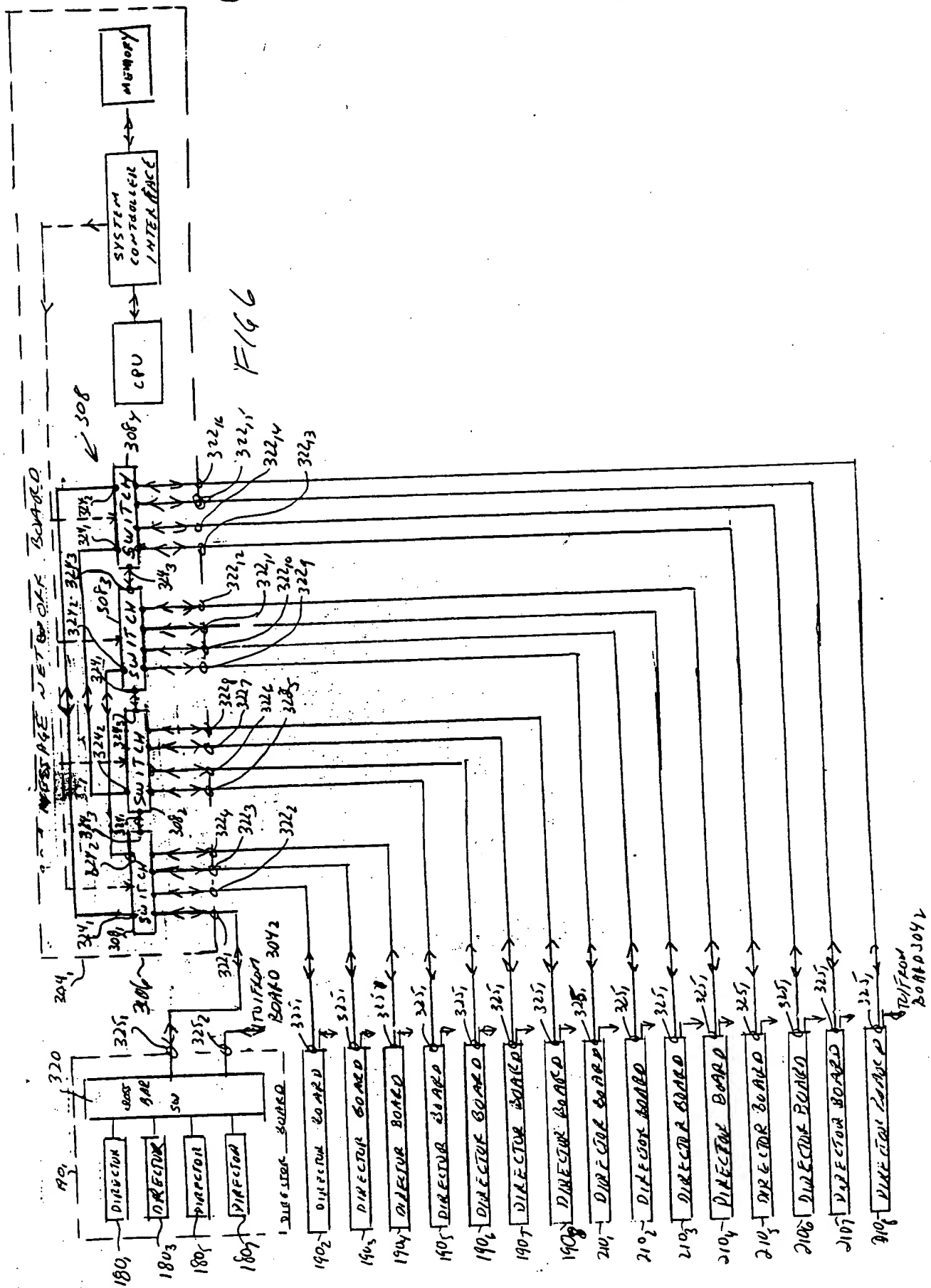
[illegible]

FIG. 7

DIRECTOR BOARD 1801

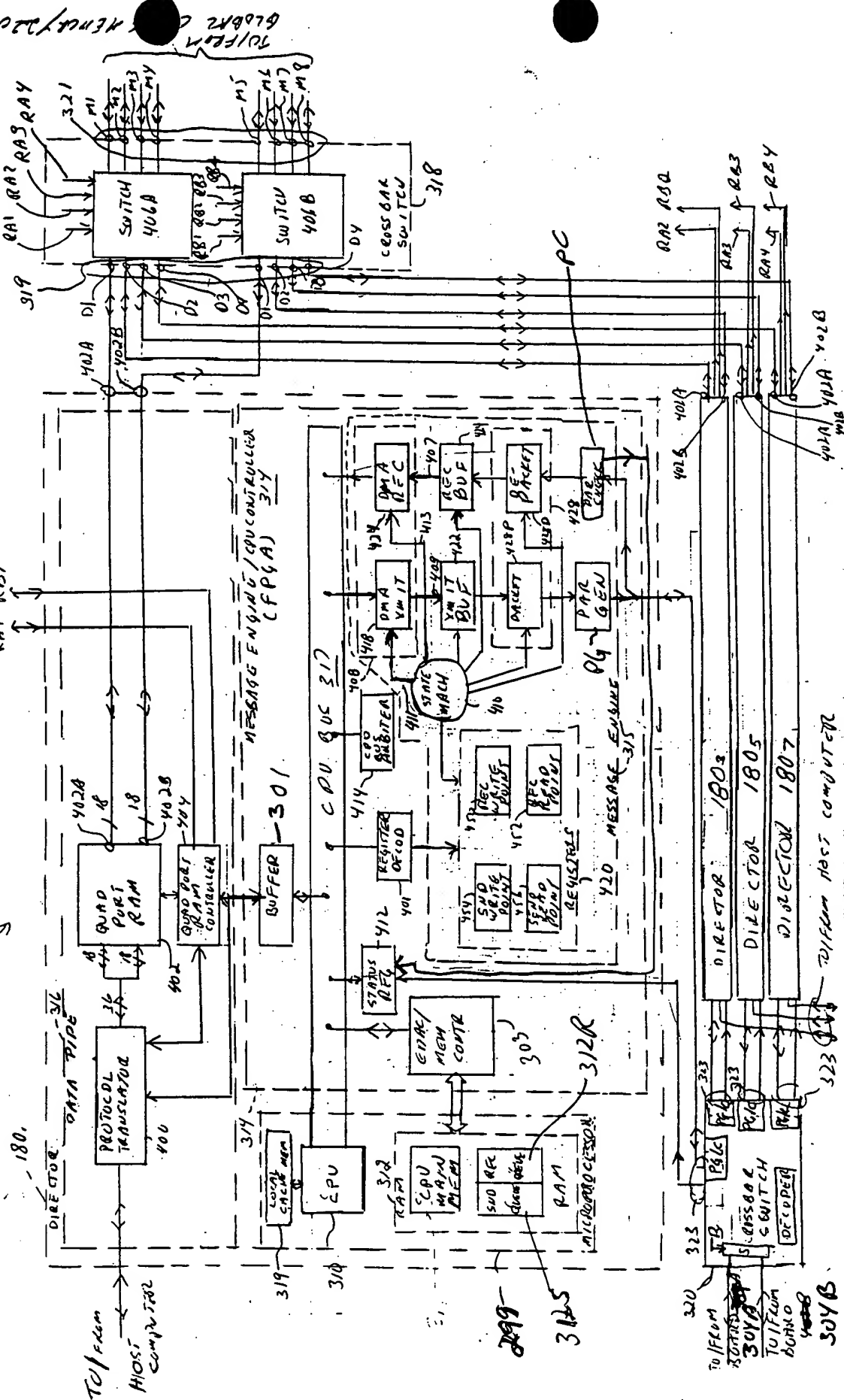
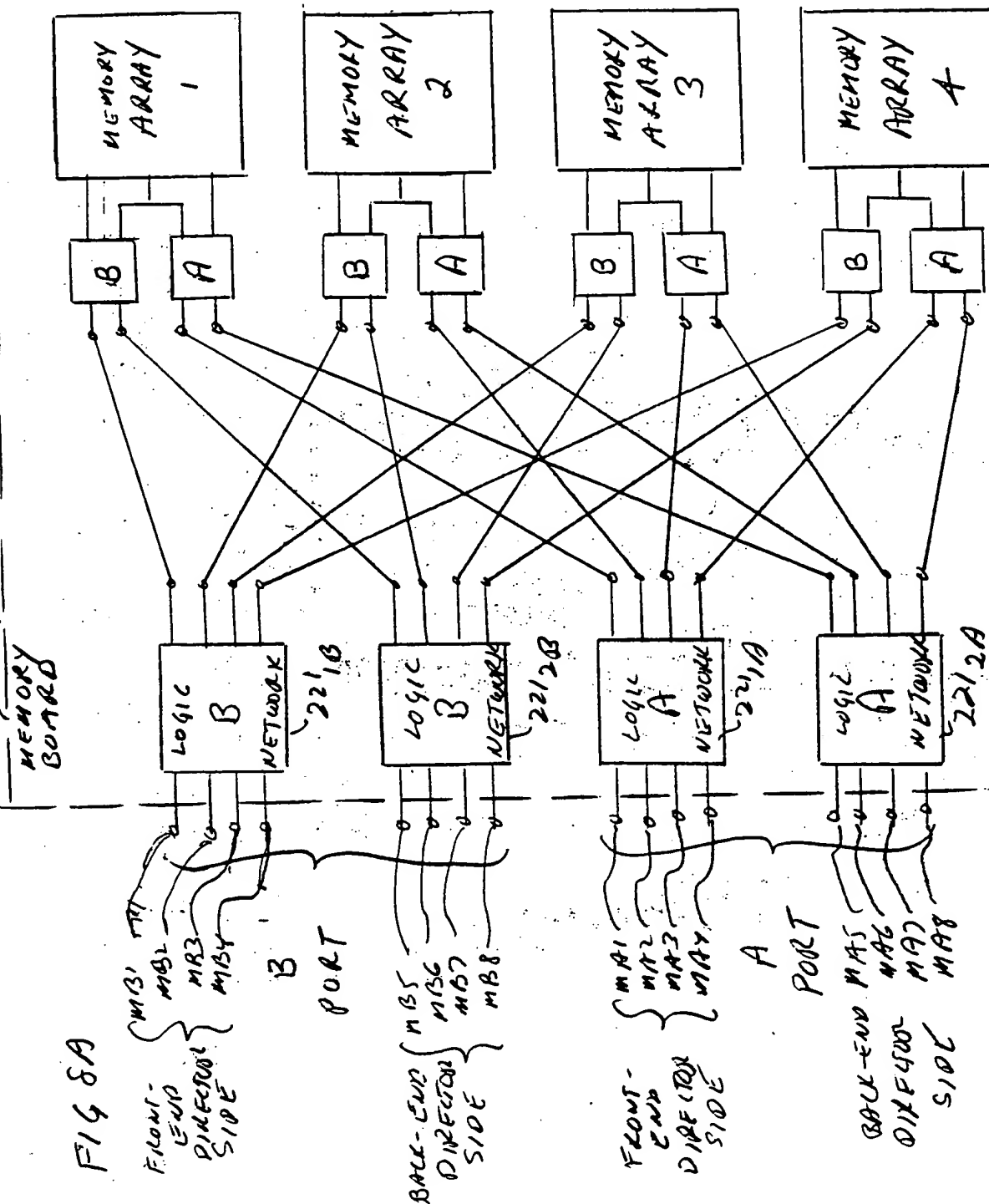




FIG 8A



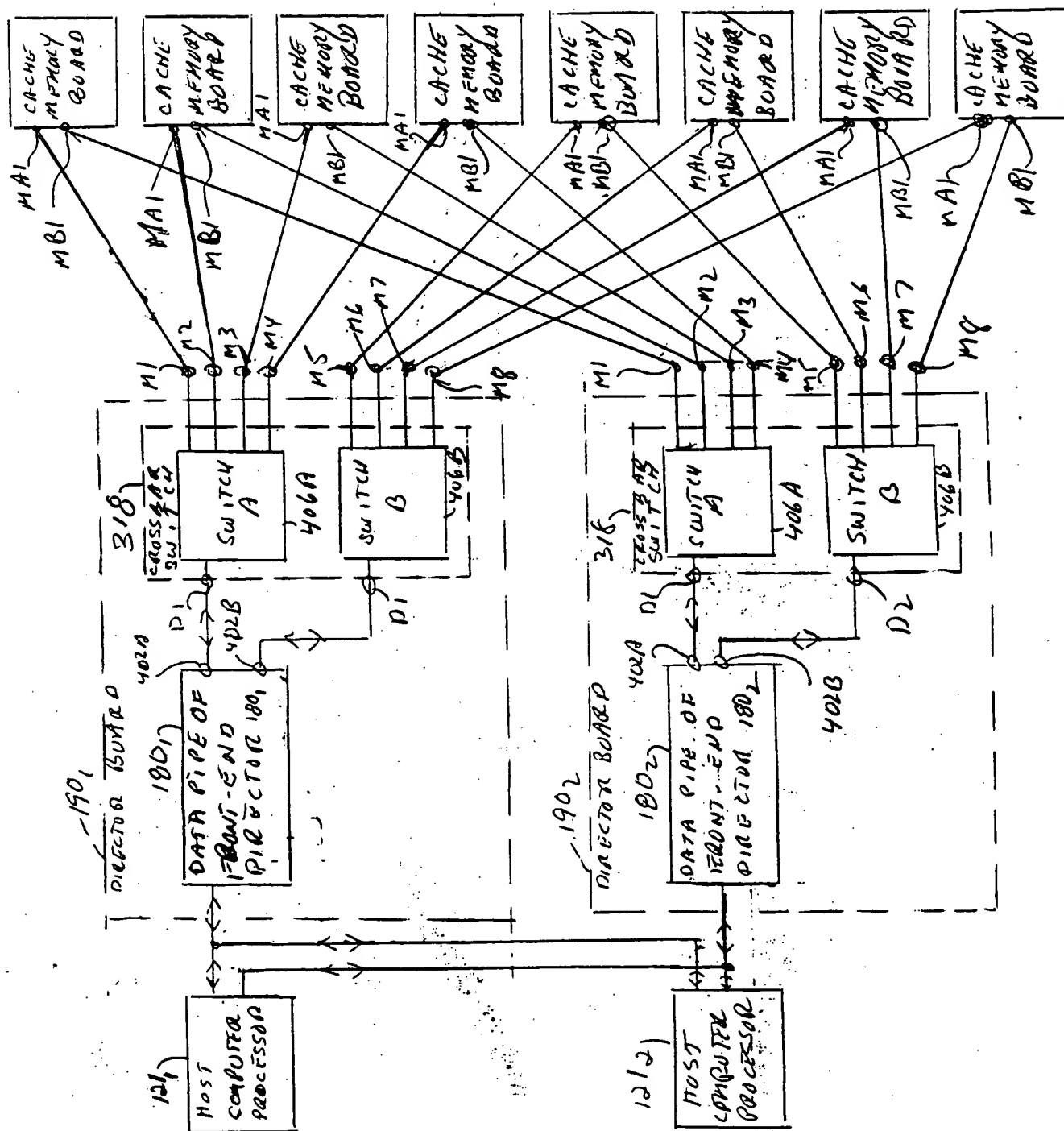
[illegible]

FIG. 8C

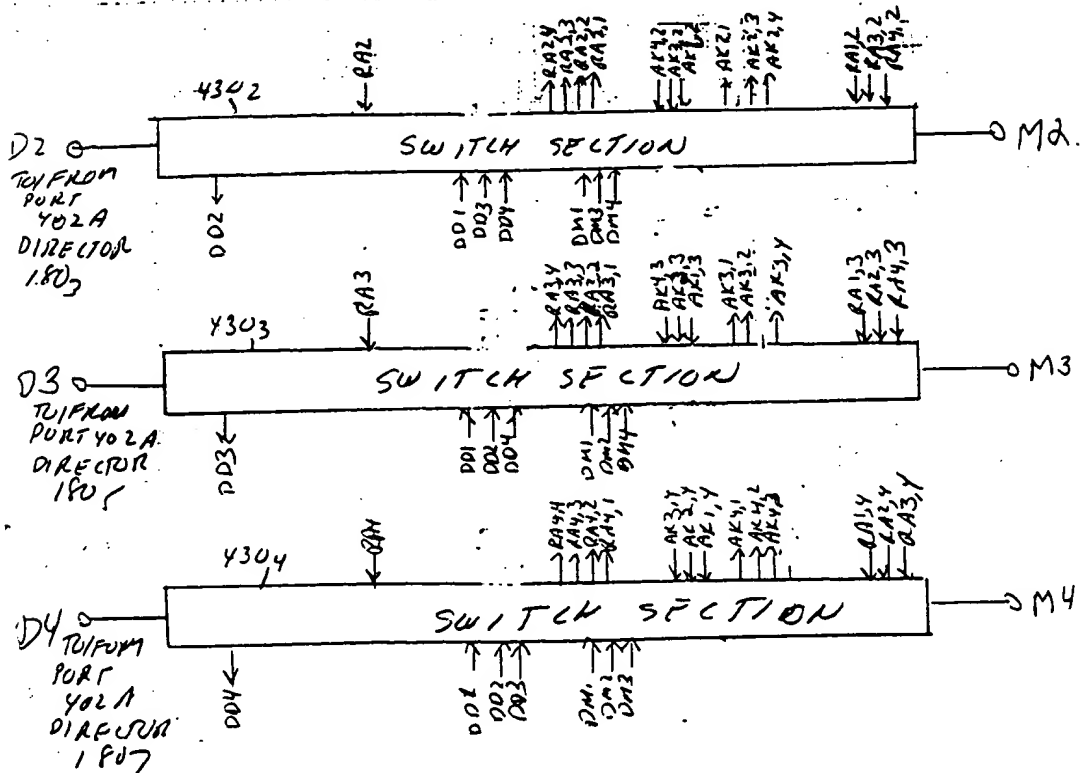
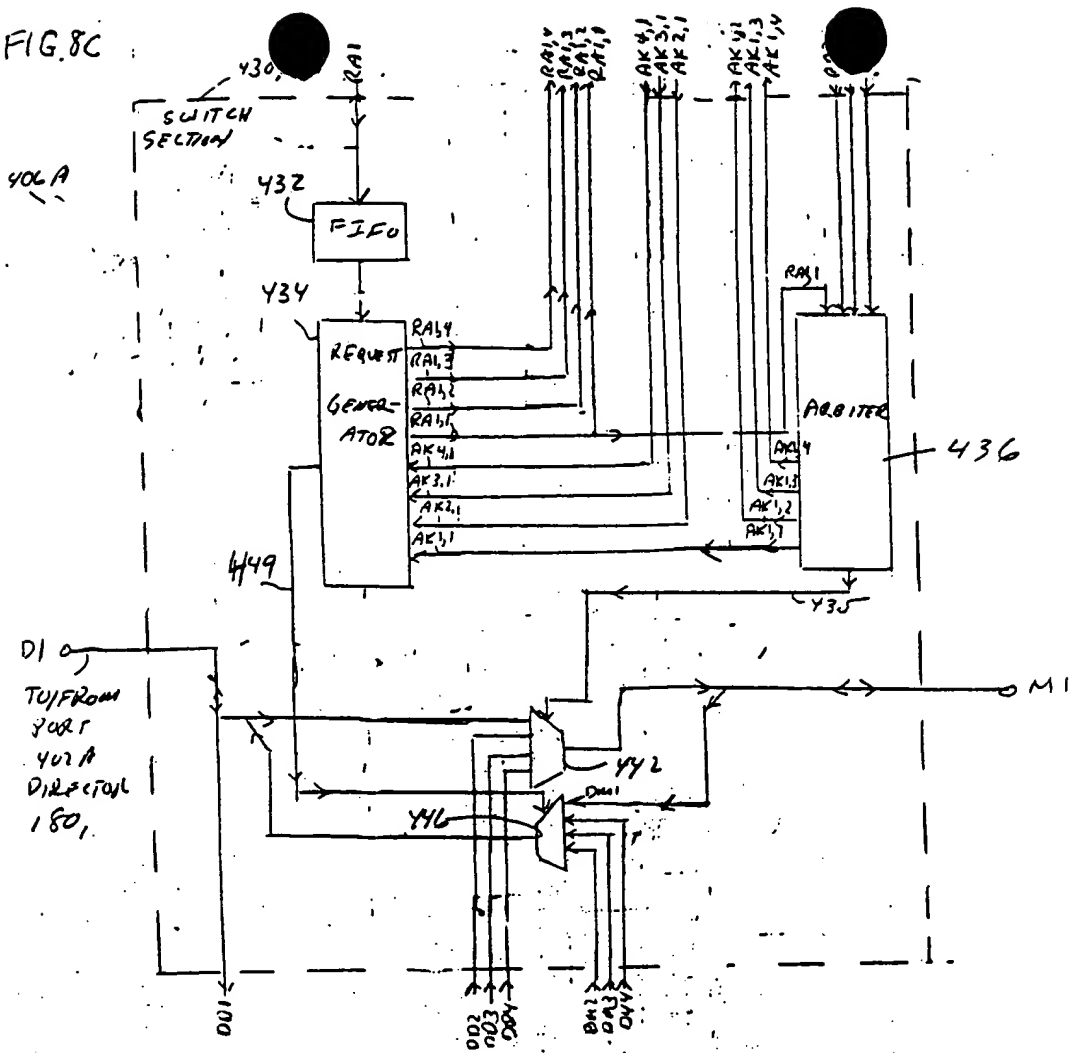
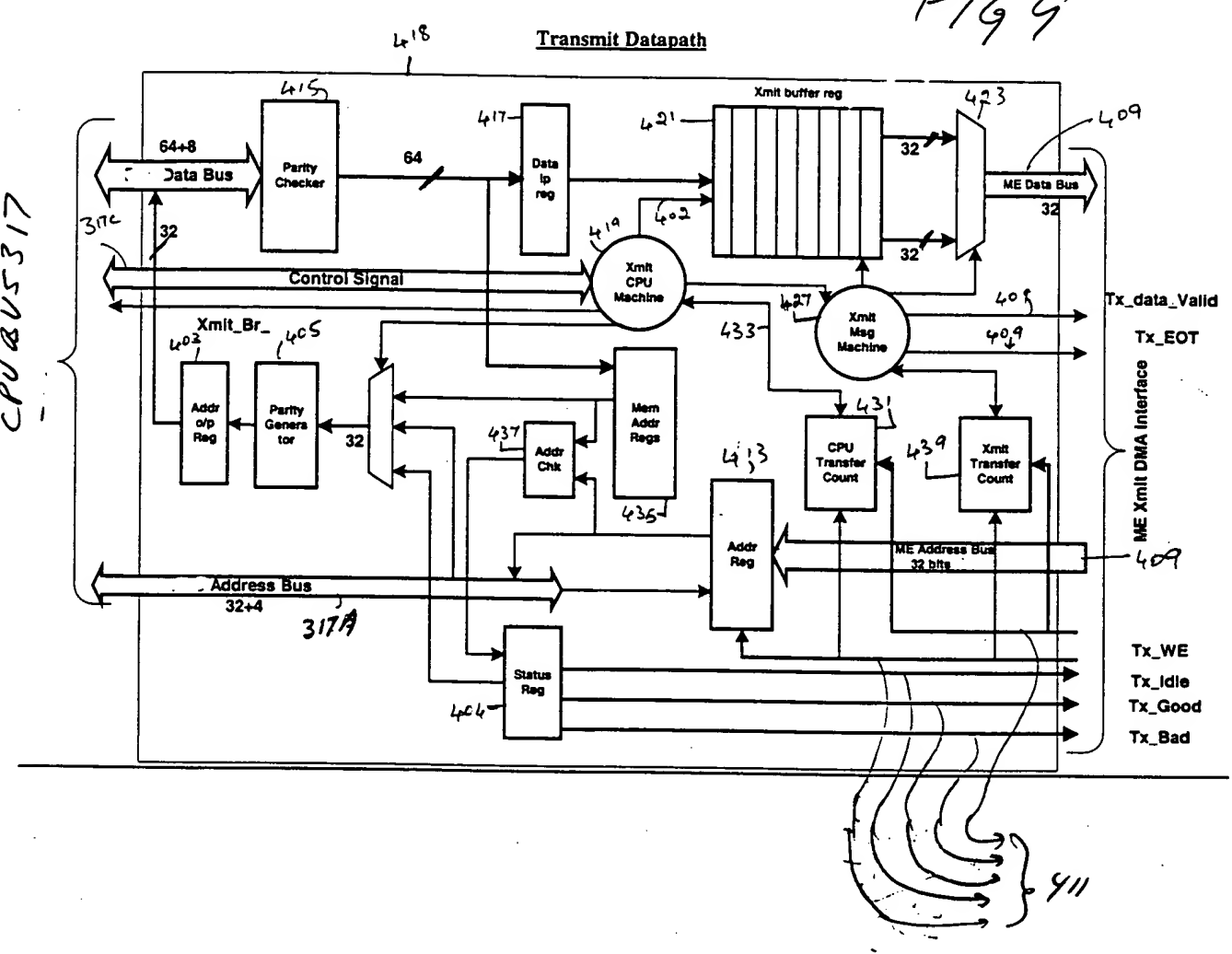


FIG 9

CPU BUS 317

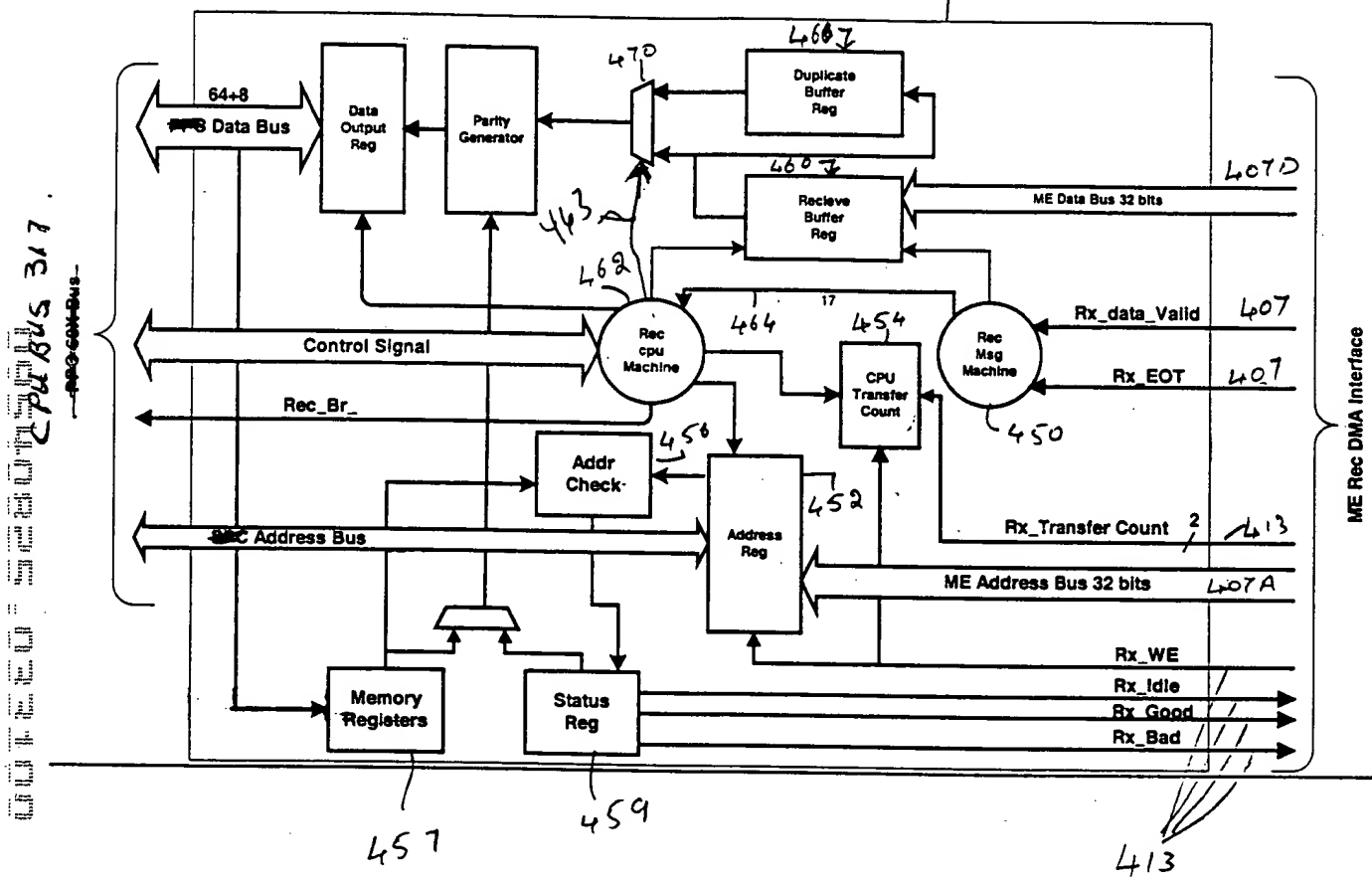
Transmit Datapath



F1610

420

Receive Datapath



Message Bus Send Operation

FIG. 11A

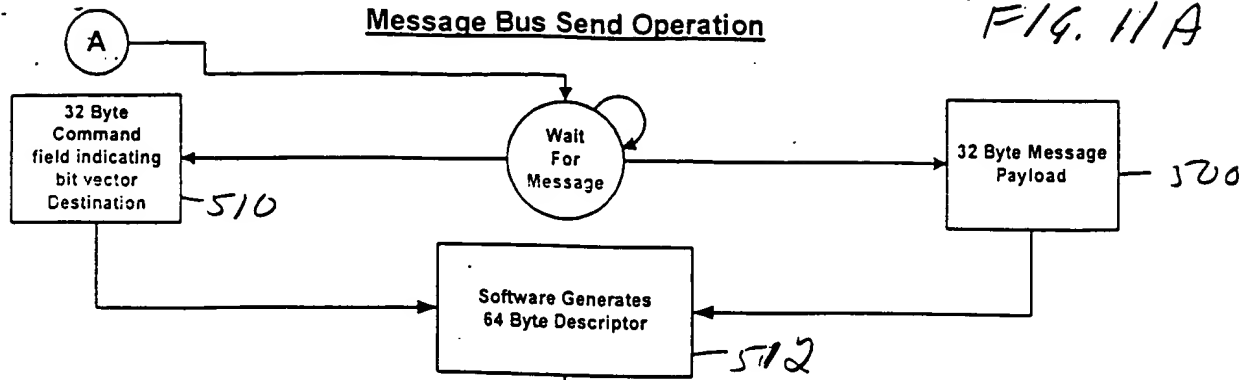
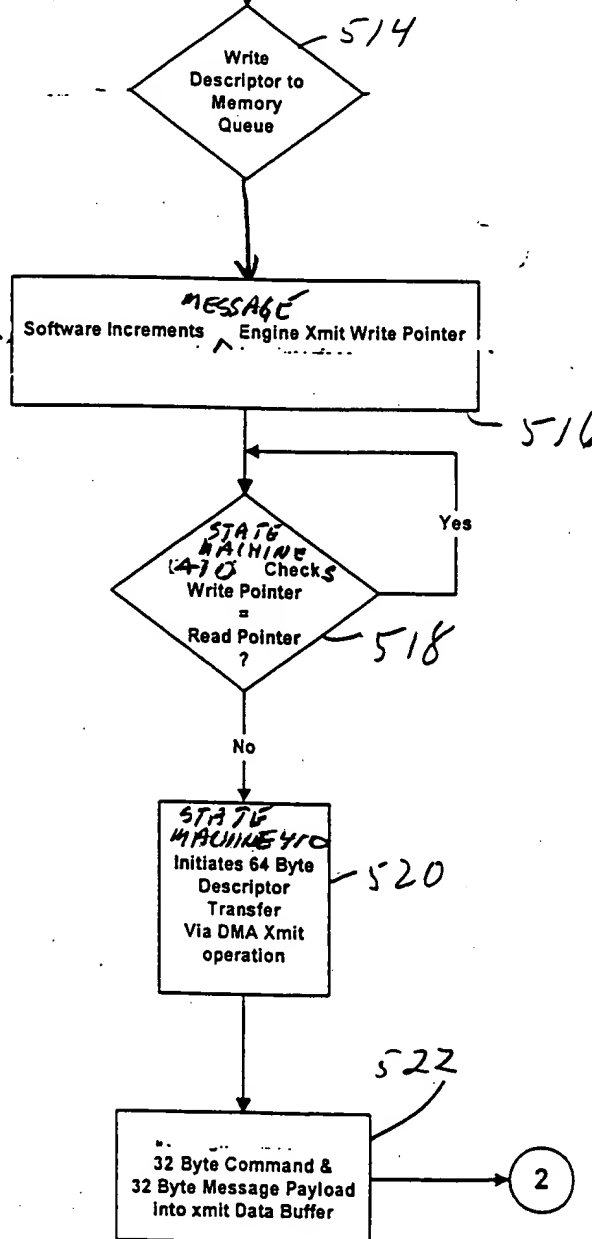


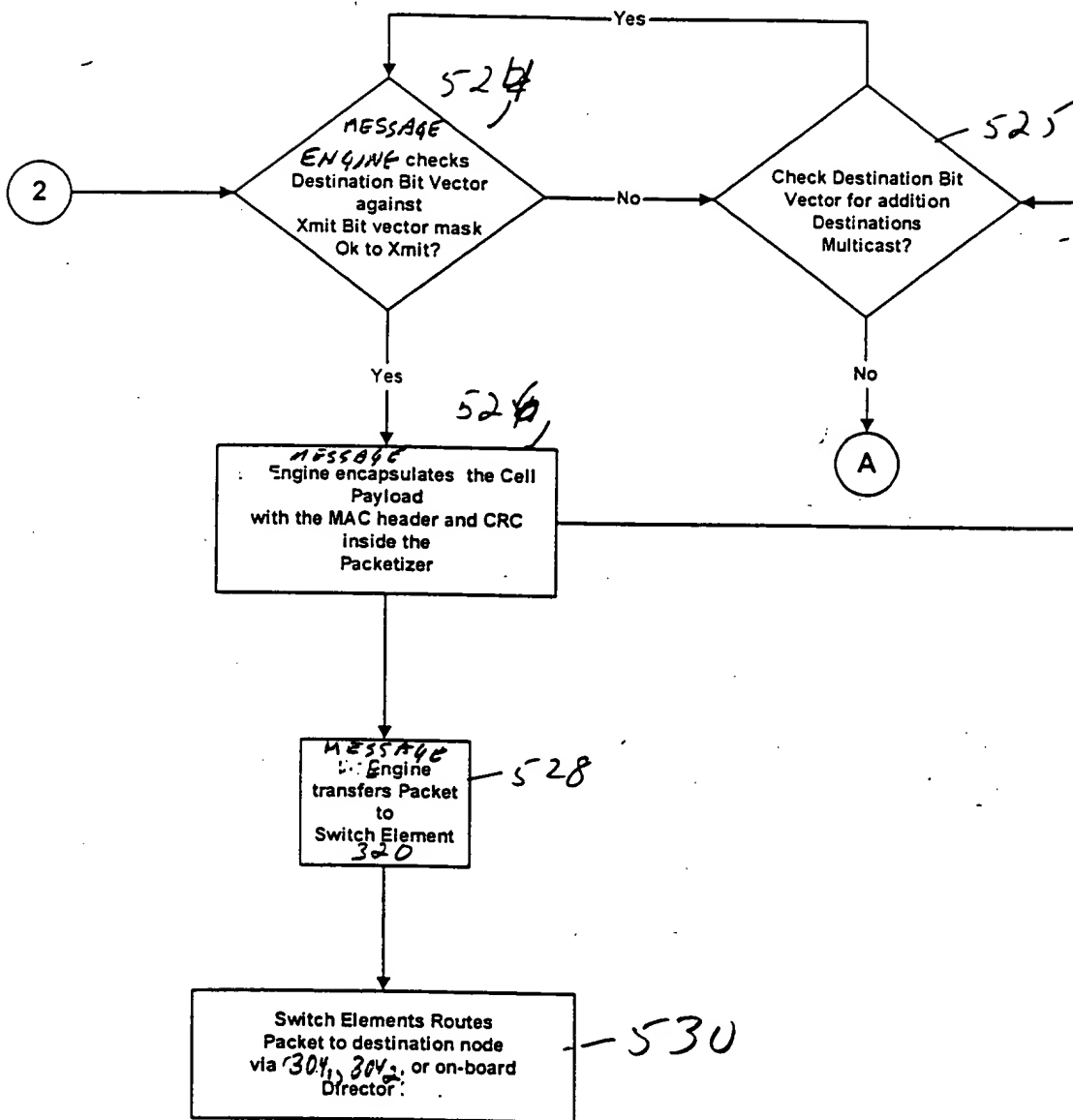
FIG 11

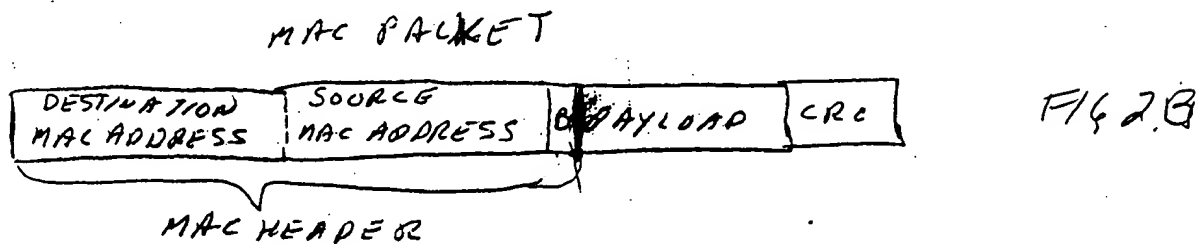
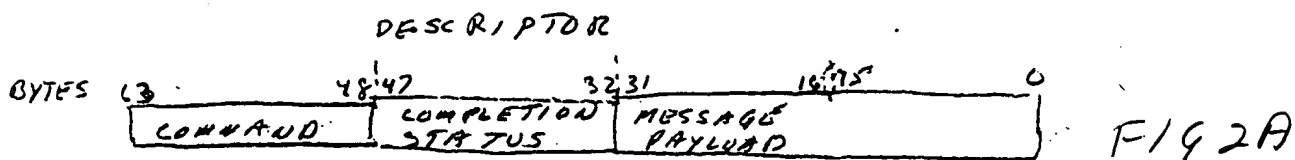
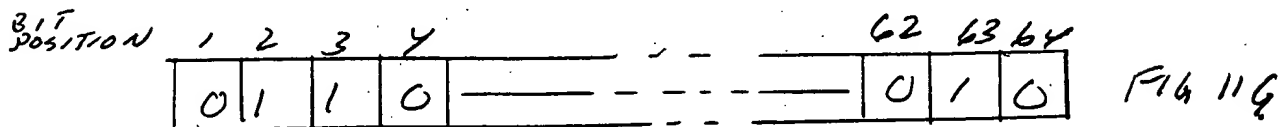
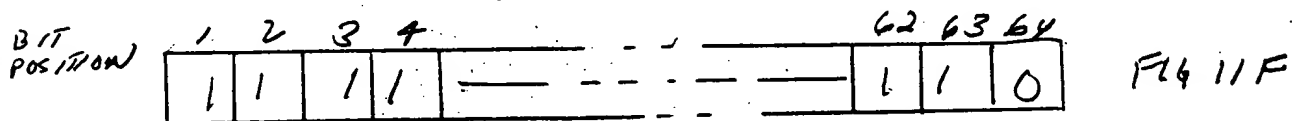
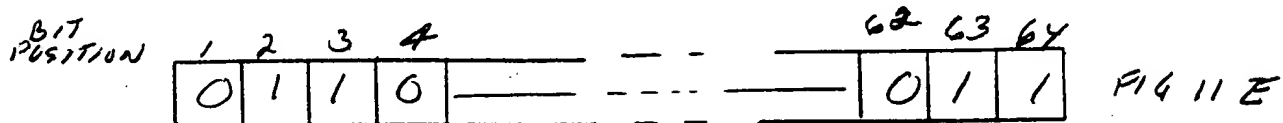
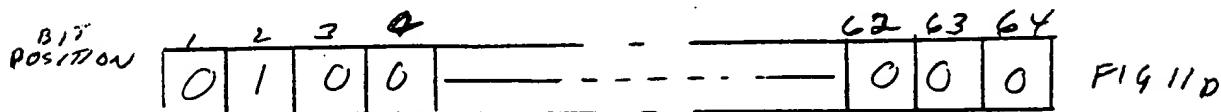
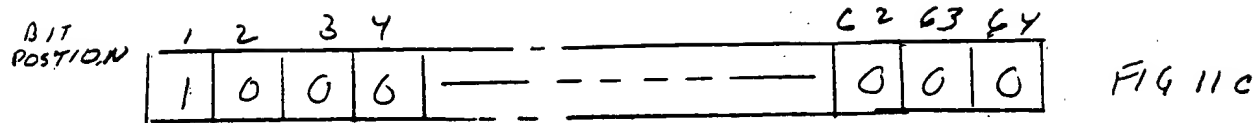
FIG 11A  
FIG 11B



Message Bus Send Operation Continued

F16 11B





# Message Bus Receive Operation

FIG. 12A

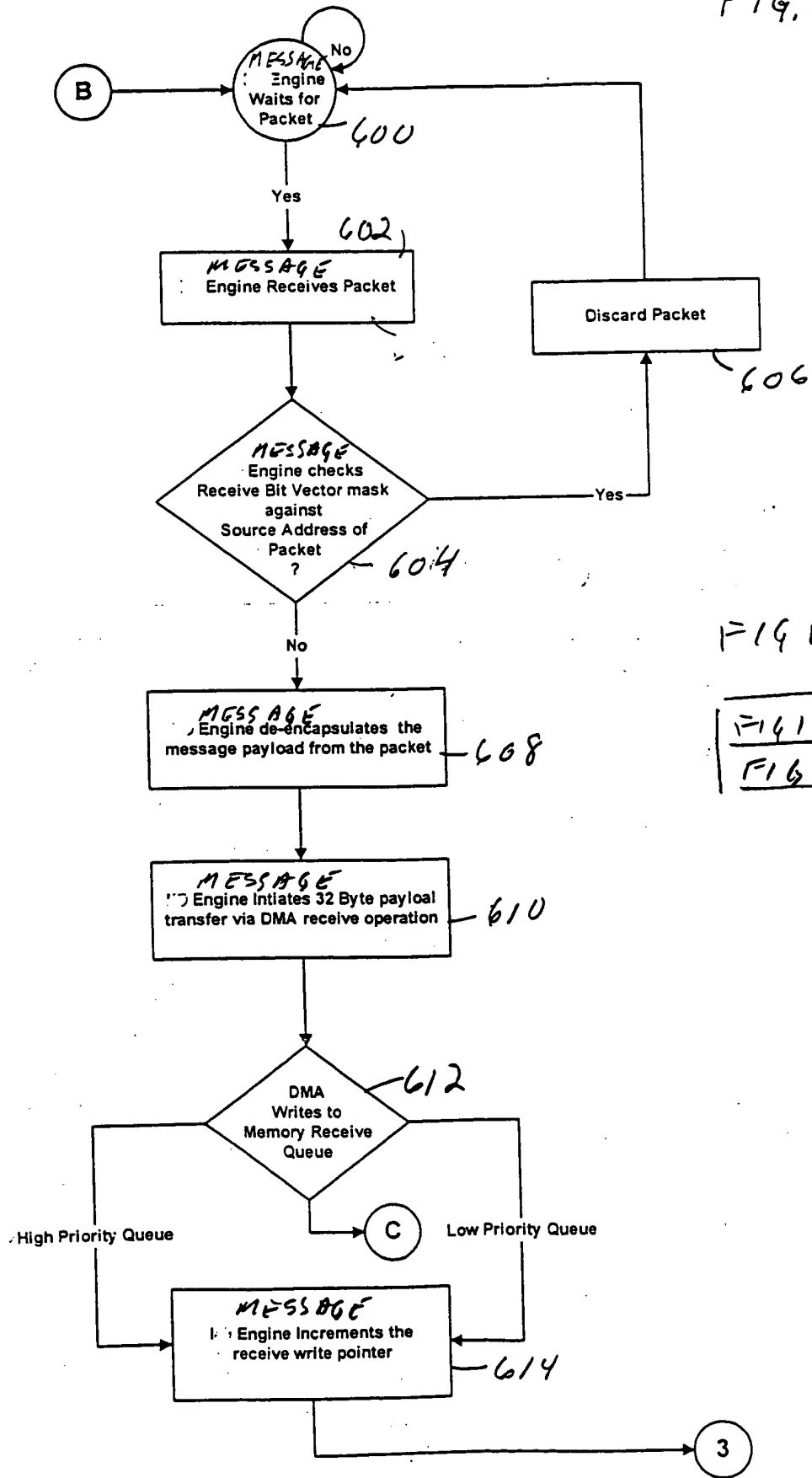
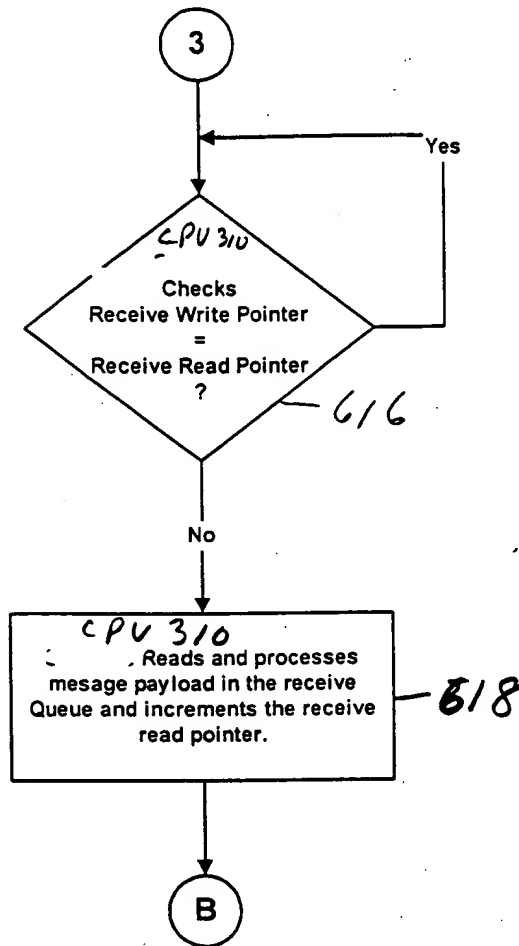


FIG 12

FIG 12A  
FIG 12B

Message Bus Receive Operation Continued



## Message Bus Acknowledgement Operation

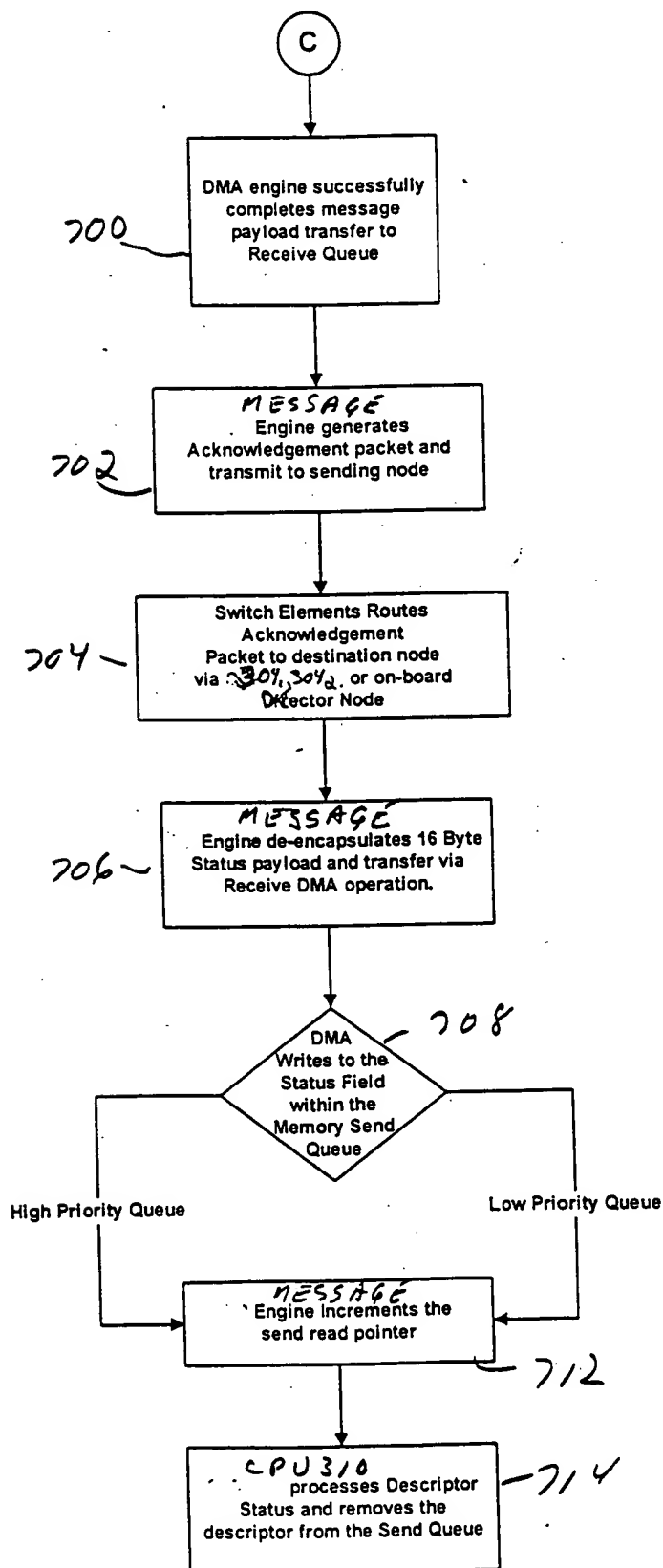
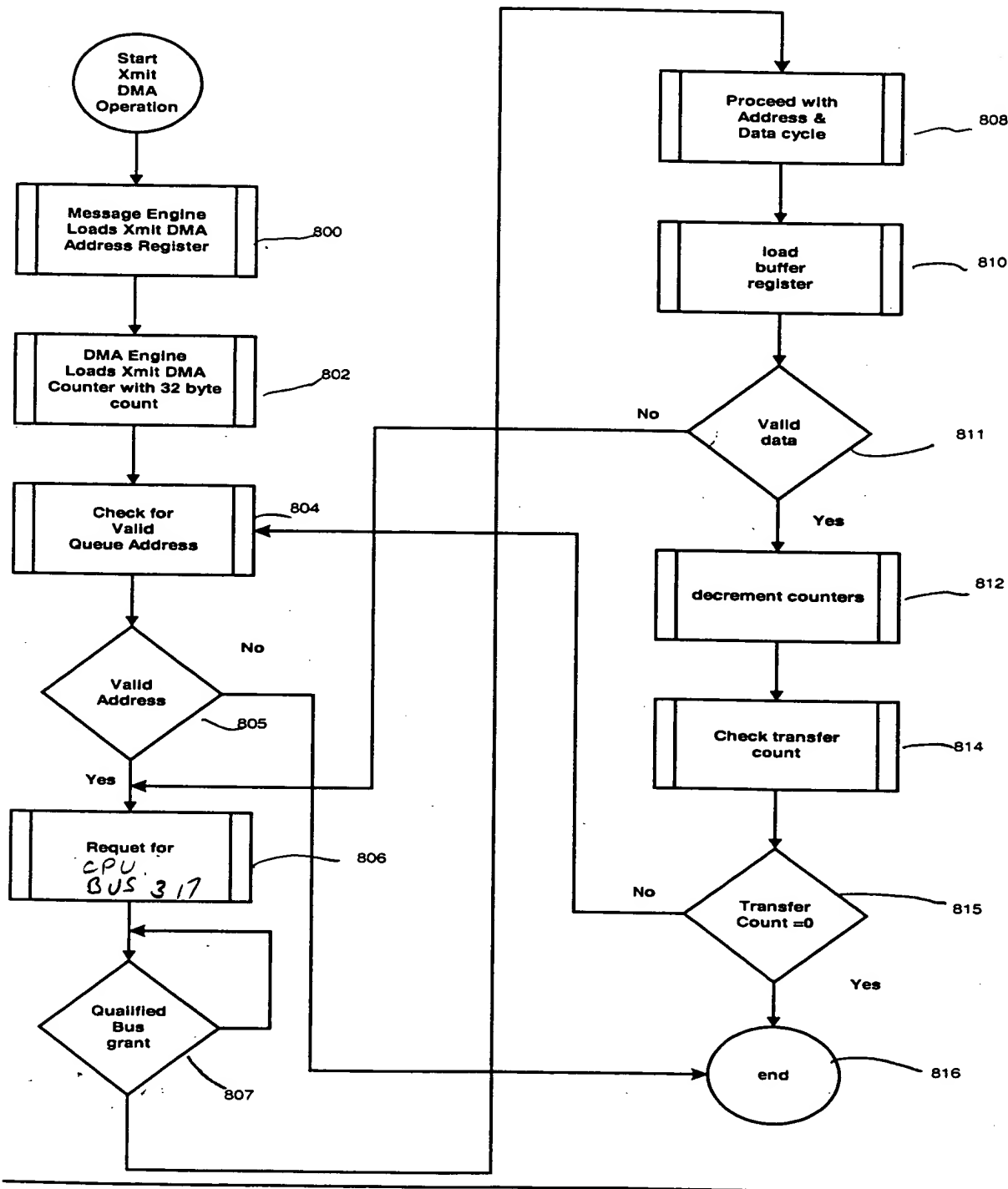


FIG 1A

Xmit CPU flow



F1414B

Xmit Msg flow

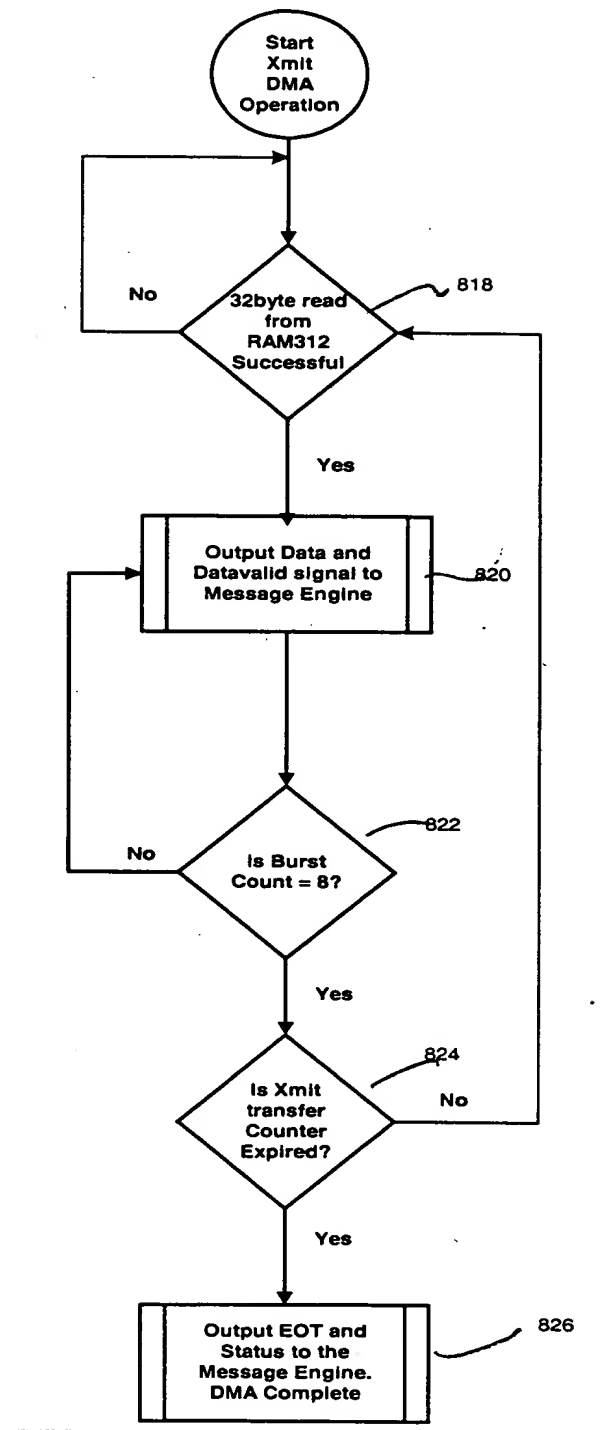
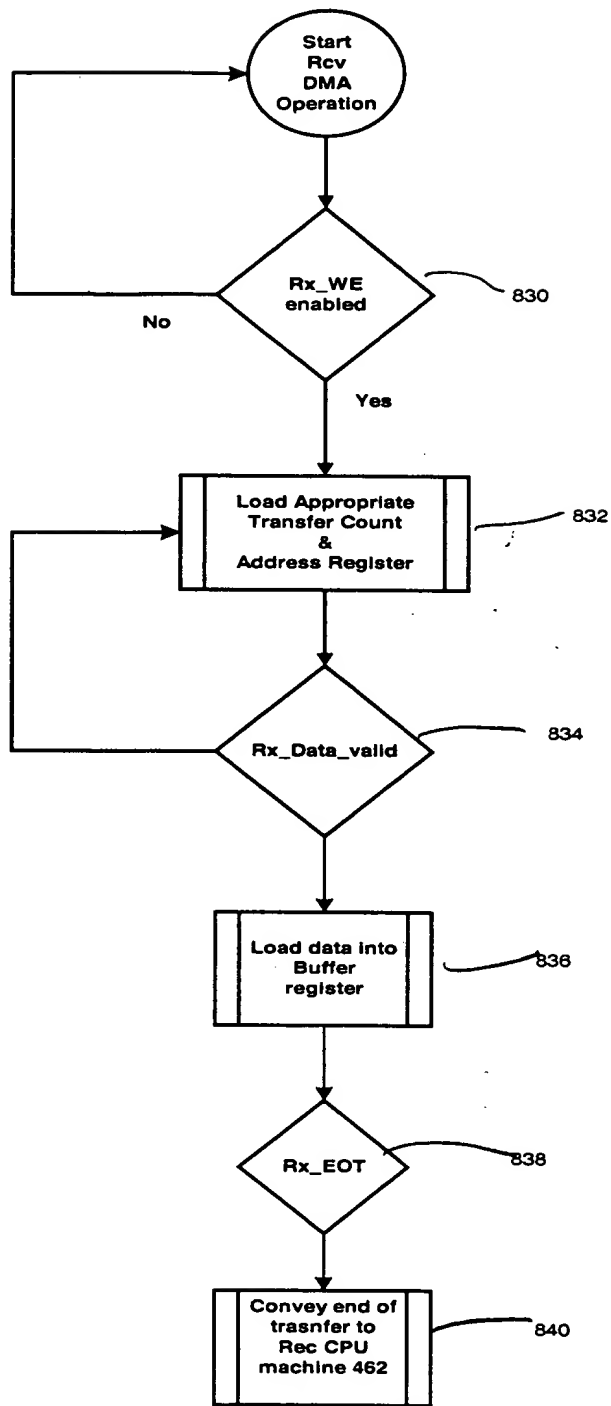


Fig 15A

Rec msg flow



F1615B

Rec cpu flow

